

REMARKS

Please find enclosed for the Examiner's approval, a proposed drawing correction with all changes made in red ink. This included inserting reference numbers 71 and 73 in Figure 14, as required by the Examiner. However, it should be noted that reference number 75 is already included in Figure 16. In view of this, it is respectfully submitted that the drawings are no longer objectionable.

Claims 31, 38-39 and 42 have also been amended, as required by the Examiner. Therefore, it is respectfully submitted that the claims are no longer objectionable.

Claims 1-6, 8-19, 22-26, 40 and 45-46 stand rejected under 35 USC 102 as being anticipated by Ueno et al. Claims 7 and 20 stand rejected under 35 USC 103 as being unpatentable over Ueno et al. in view of Guetz et al. Claims 27-32, 34-39 and 47 stand rejected under 35 USC 103 as being unpatentable over Ueno et al. in view of Lempel, Claim 33 stands rejected under 35 USC 103 as being unpatentable over Ueno et al. in view of Lempel, and in further view of Guetz et al. Based on the following, these rejections are respectfully traversed.

Previously, the Applicant has respectfully pointed out that the claims recite features not taught by Ueno et al.

In particular such features include "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks", as recited in claims 1, 14, 27 and 40. However, despite this point, the above rejections have been maintained.

In maintaining the above rejections, the upsampling circuit 35 shown in Figure 7 of Ueno et al. is being relied. In maintaining these rejections, it was also stated that the low resolution local decoded signal 34 output from the local decoder 33 as shown in Figure 7 of Ueno et al. is actually based on first blocks of pixels in the reference frame and one or more blocks of pixels that substantially correspond to the first block of pixels as provided by the search range calculation within coding section 30 of Figure 7 of Ueno et al. (See column 14, lines 33-41, column 16, lines 8-20).

However, the Applicant has carefully reviewed the above portions and does not see where it supports the above interpretation of Ueno et al. In fact, these portions of Ueno et al. do not even mention the upsampling circuit 35, local decoder 33 and coding section 30 of Figure 7, as mentioned above.

Moreover, in column 19, lines 41-54, Ueno et al. discloses a signal obtained by horizontal upsampling...is

separated into an odd-field signal and even-field signal in a first field separator 402. Ueno et al. further discloses that the odd-field signal and even-field signal are subjected to vertical interpolation.

Based on the above disclosure, it is evident that the up-sampling of Ueno et al. does not perform "determining values of additional pixels based on values of pixels in the first block and on values of pixels in the one or more blocks", as required by the claims. Therefore, it is respectfully submitted that this feature is distinguishable over Ueno et al.

The above-described deficiencies of Ueno et al. are also not addressed by either Lempel or Guetz et al. since they are being relied on for other features. Thus, the invention of Claims 1-7, 9-20, 22-33, 35-40 and 45-47 is neither anticipated nor made obvious by Ueno et al. alone or in combination with either Lempel or Guetz et al. Therefore, it is respectfully requested that these rejections be reconsidered and withdrawn.

Claims 42-43 stand rejected under 35 USC 102 as being anticipated by Yonemitsu et al. Claim 44 stands rejected under 35 USC 103 as being unpatentable over Yonemitsu et al. in view of Song et al. Based on the following, these rejections are respectfully traversed.

In response to the above rejections, it is respectfully submitted that the claims recite features not taught by Yonemitsu et al. In particular such features include "a processor which increases a resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of the video", as recited in claim 42.

In addressing this feature in the above rejections, the up sampling circuit 57 of Yonemitsu et al. is being relied on. However, in column 7, lines 11-13, Yanemitsu et al. discloses that the lower layer is input to the up sampling circuit 57, in which it is processed by interpolation so that its converted into a non-interlace picture.

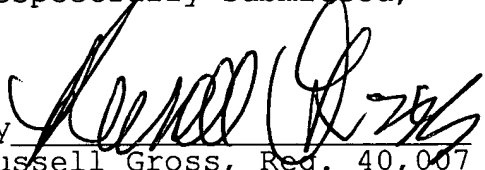
Based on the above disclosure, it is evident that the up sampling circuit 57 of Yonemitsu et al. does not "increase a resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of the video", as required by the claims. Therefore, it is respectfully submitted that this feature is distinguishable over Yonemitsu et al.

The above-described deficiencies of Yonemitsu et al. are also not addressed by Song et al. Thus, the invention of claims 42-44 is neither anticipated nor made Yonemitsu

et al. alone or in combination with Song et al. Therefore,
it is respectfully requested that these rejections be
reconsidered and withdrawn.

The Commissioner is hereby authorized to credit any
overpayment or charge any fee (except the issue fee) to
Account No. 14-1270.

Respectfully submitted,

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On June 25, 2002

By Elena Chapa

A P P E N D I X

31. (TWICE AMENDED) An apparatus~~method~~ according to claim 30, wherein the differences comprise a residual.

38. (AMENDED) An apparatus~~method~~ according to claim 27, wherein the processor uses motion vectors from the reference frame to the target frame to locate the one or more blocks of pixels.

39. (AMENDED) An apparatus~~method~~ according to claim 27, wherein the processor searches through N target frames to locate the one or more blocks of pixels.

42. (TWICE AMENDED) A television system which receives coded video data, and which forms images based on the coded video data, the television system comprising:

- a decoder which decodes the video data to produce frames of video;

- a processor which increases a resolution of a reference frame of the video based on pixels in the reference frame and based on pixels in at least one other target frame of the video; and

- a display which displays an image based on the reference frame;

wherein the processor increases the resolution of the reference frame by selecting blocks of pixels in the reference frame and, for each selected block, (i) locating, in N ($N \geq 3$) target frames, one or more blocks of pixels that substantially correspond to the first block of pixels, where the N target frames are separate from the reference frame; (ii) determining values of additional pixels based on values of pixels in the selected block and on values of pixels in the one or more blocks, and (iii) adding the additional pixels among the pixels in the selected block.

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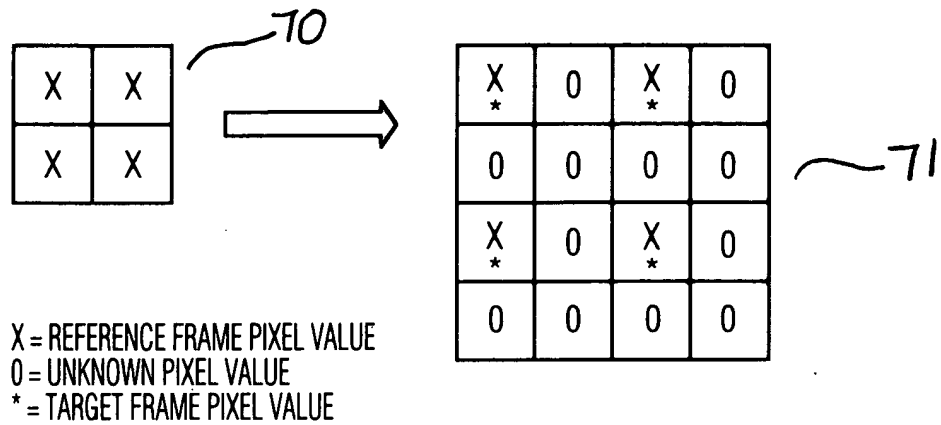


FIG. 13

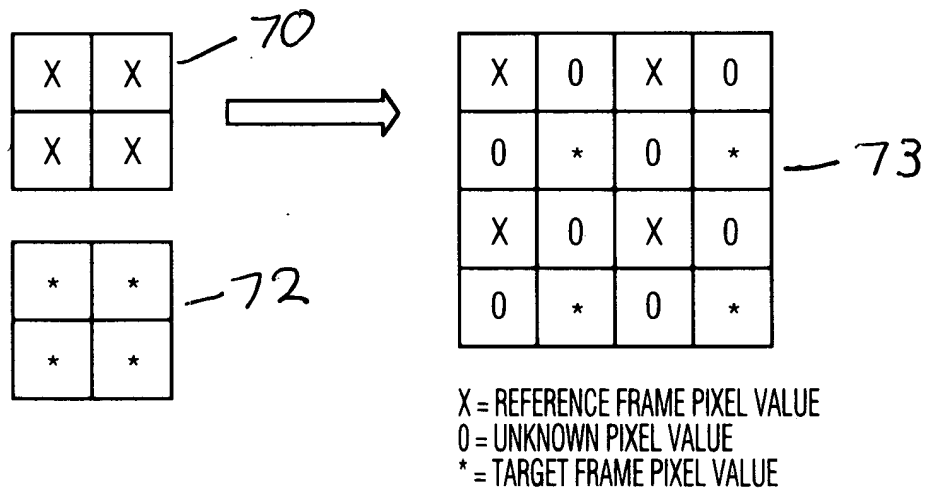


FIG. 14